800Gb/s QSFP-DD SR8 Transceiver

S-QS800G85DM1201-CD

Product Features

- ► Hot-pluggable QSFP-DD form factor
- ► VCSEL transmitter and PIN PD receiver
- ► Support 850Gb/s aggregate bit rate
- ► Compliant with IEEE802.3df-2024:-8x100GBASE-SR1/4x200GBASE-SR2/ 2x400GBASE-SR/1x800GBASE-SR8 optical interface
- ► Compliant with IEEE 802.3df-2024:-8x100GAUI-1/4x200GAUI-2/2x400GAUI-4/ 1x800GAUI-8 C2M electrical interface
- ► Compliant with QSFP-DD MSA Hardware Rev 7.0
- ► Type 2B housing with Dual MPO-12/APC receptacle
- ► Compliant with CMIS Rev 5.0
- ► Case operating temperature 0°C to 70°C
- ► Power dissipation < 16W
- ► Two wire serial Interface with digital diagnostic monitoring
- ► Complies with EU Directive 2011/65/EU (RoHS compliant)
- ► Class 1 Laser

Product Applications

- ► Data Center 800GE 100m MMF links

Performance Specifications

Absolute Maximum Ratings					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Note**
Storage Temperature	Ts	-40	85	ºC	
Relative Humidity	RH	5	85	%	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Signal Input Voltage		Vcc-0.3	Vcc+0.3	V	
Data Input Voltage Differential	$\lvert V_{DIP}-V_{DIN}\rvert$	-	1	V	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	
Control Output Current	I_O	-20	20	mA	

Recommended Operating Conditions						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot	I_{CC_IP}	-	-	6400	mA	

plug						
Sustained peak current at hot plug	I_{CC_SP}	-	-	5328	mA	
Maximum Power Dissipation	P_D	-	-	16	W	
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	2	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	VIH	V_{CC}*0.7	-	V_{CC}+0.3	V	
Control Input Voltage Low	VIL	-0.3	-	V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	-	-	50	m	1
Note 1: 0.5 m to 30 m for OM3, 0.5 m to 50 m for OM4 and OM5, with FEC.						

Optical Characteristics

Transmitter

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Signaling rate, each lane (range) 100G-SR1, 200G-SR2, 400G-SR4 800G-SR8,PMDs	-	53.125 ± 100 ppm 53.125 ± 50 ppm			GBd	
Wavelength	λ_C	844	-	860	nm	
RMS spectral width	RMS	-	-	0.6	dB	1
Average Launch Power, each lane	AOP_L	-4.6	-	4.0	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane for max (TECQ, TDECQ) <= 1.8 dB for 1.8 < max (TECQ, TDECQ) <= 4.4 dB	OMAouter	-2.6 -4.4+max(TECQ, TDECQ)	-	3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	4.4	dB	2
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ	-	-	4.4	dB	
Over/under-shoot	-	-		29	%	
Transmitter power excursion, each lane	-	-		2.3	dBm	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-30	dBm	
Extinction Ratio, each lane	ER	2.5	-	-	dB	
Transmitter transition time, each lane	Tr	-	-	17	ps	

RIN14OMA	RIN			-132	dB/Hz	
Optical return loss tolerance	ORL			14	dB	
Encircled flux	-	>=86% at 19 μ m <=30% at 4.5 μ m			-	-

Optical Characteristics

Receiver

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Signaling rate, each lane (range) 100G-SR1, 200G-SR2, 400G-SR4 800G-SR8,PMDs	-	53.125 ± 100 ppm 53.125 ± 50 ppm			GBd	
Wavelength	λ_C	840	-	860	nm	
Damage Threshold, each Lane	AOP_D	5	-	-	dBm	
Average Receive Power, each Lane	AOP_R	-6.4	-	4	dBm	
Receive Power (OMAouter), each Lane	OMA_R	-	-	3.5	dBm	
Receiver Reflectance	RR	-	-	-15	dB	
Receiver Sensitivity (OMAouter), each Lane	S_{OMA}	-	-	-4.6 -6.4+TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-2	dBm	3
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	4.4	-	dB	
OMAouter of each aggressor lane	-	-	3.5	-	dBm	

Note：

1. RMS spectral width is the standard deviation of the spectrum.
2. Only support 33.6GHz 3 dB bandwidth of the fiber emulation filter for TDECQ measurement.
3. Measured with conformance test signal at TP3 for the BER = 2.4x10-4.

Functional Characteristics (Electrical)

Receiver (Module Output, TP4)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Peak-to-peak AC common-mode Voltage Low-frequency, VCMLF Full-band, VCMFB	-	-	-	 32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode Disabled	-	-	-	 600 845 35	mV	

Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
Transmitter (Module Input, TP1)						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	-	 32 80	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

Electrical Specification Low Speed Control and Sense Signals					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Notes**
Module output SCL and SDA	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC} -0.5	V_{CC}+0.3	V	

Digital Diagnostics				
Parameter	**Range**	**Accuracy**	**Unit**	**Calibration**
Temperature	0 to 70	±3	℃	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 15	10%	mA	Internal
Tx Output Power (Each Lane)	-4.6 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-6.4 to +4	±3	dB	Internal

Pin Definitions and Functions

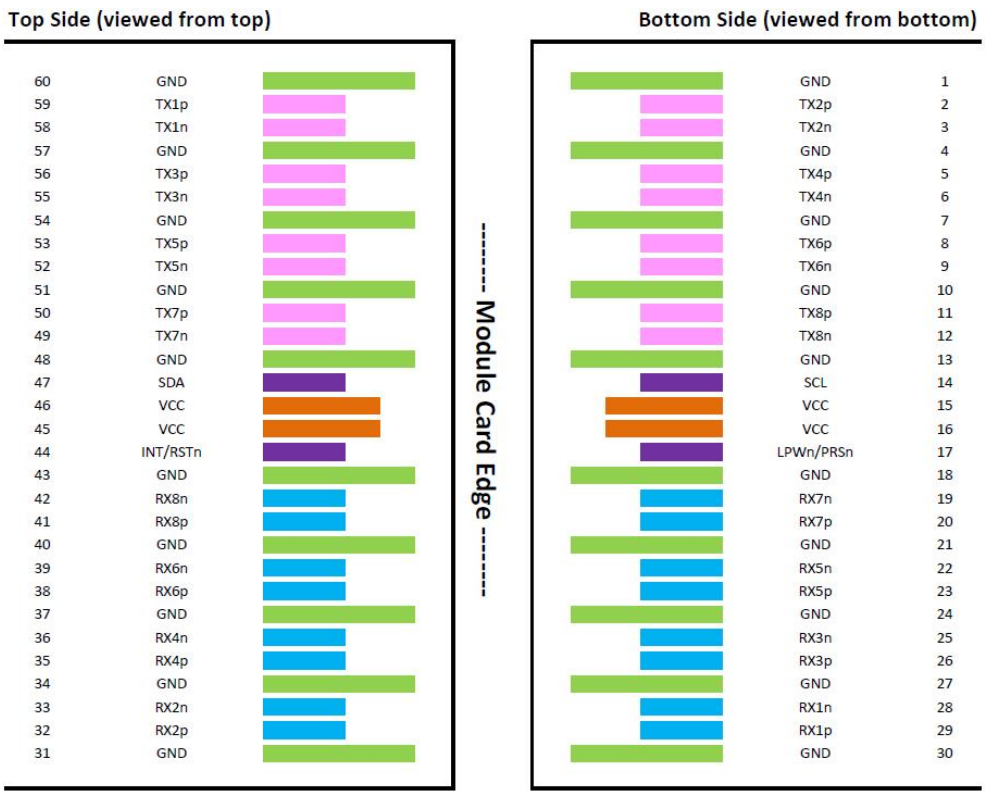
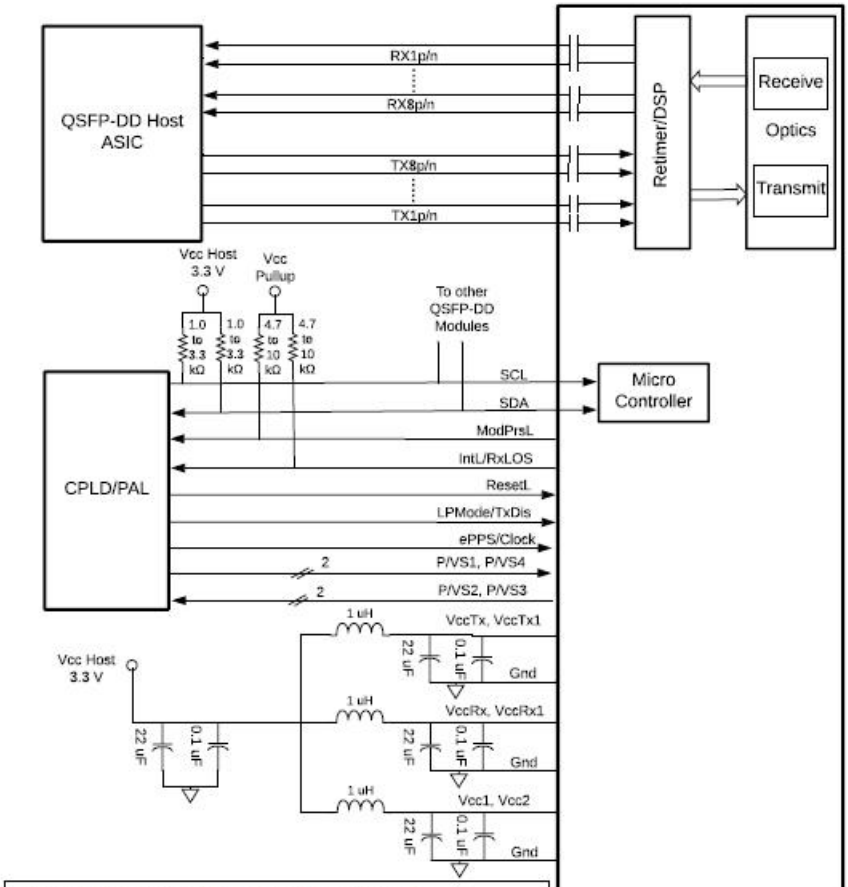


Figure 1 – Pinout definitions of OSFP module inputs/outputs

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS/ CML-I	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS -I/O	SCL	TWI serial interface clock	49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS -I/O	SDA	TWI serial interface data	50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	51		GND	Ground

14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	66		Reserve d	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	69	LVCMO S-I	ePPS/Clo c k	1PPS PTP clock or reference clock input
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

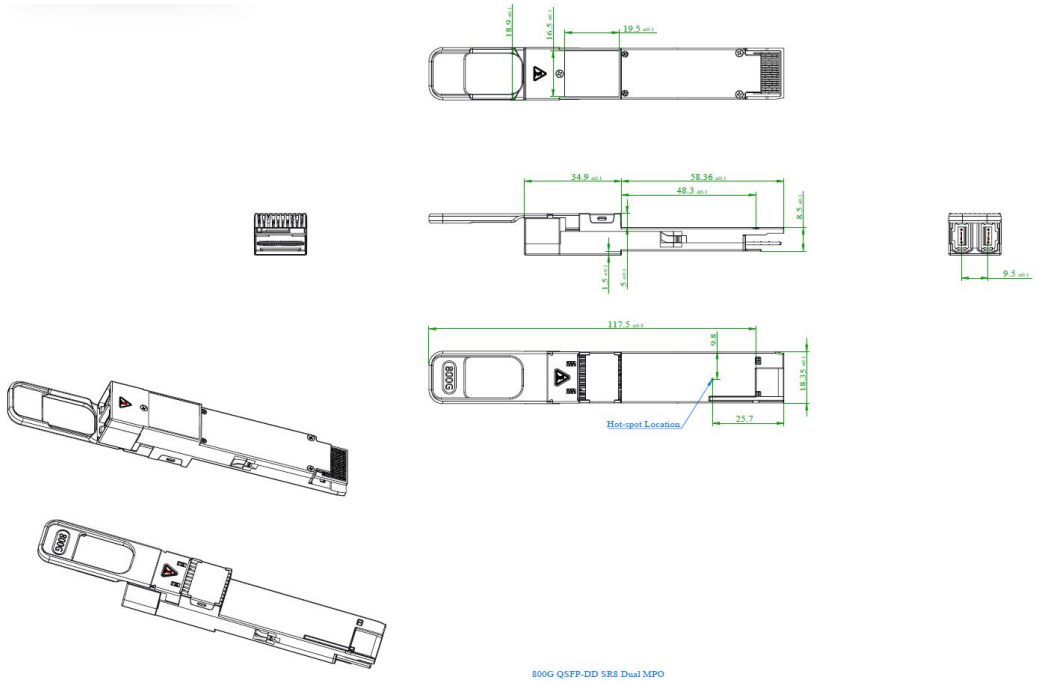
Recommended OSFP Host Board Schematic



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

Mechanical Diagram



Unit:mm

Order Information

Part Number	Description
S-QS800G85DM1201-CD	800G QSFP-DD SR8 Transceiver/0~70℃/2xMPO-12/MMF